REMARKS

Present Status of the Application

The Office Action has rejected claims 24-35 and 37-46 under 35 U.S.C. Section 103(a) as being unpatentable over Kumagai (US 2003/0218588) in view of Nakano (US 7,098,901).

Discussion of Claim Rejections

Claims 24-35 and 37-46 are rejected under 35 U.S.C. Section 103(a) as being unpatentable over Kumagai (US 2003/0218588) in view of Nakano (US 7,098,901).

The claim 24 recites "[a] source driver, ...a transmitter, coupled to said receiver, transmitter receiving said master/slave setting signal, said transmitter responsive to said master/slave setting signal operating in one of a master mode and a slave mode; wherein when said transmitter **operates in said master mode**, said transmitter **enhances a driving ability** of said clock signal, said display data, and said control signal for use of another source driver in a next stage; when said transmitter **operates in said slave mode, said transmitter directly outputs** said clock signal, said display data, and said control signal received from said receiver for use of said another source driver in said next stage."

Examiner states that Kumagai (Fig. 3 and par. [0060]) teaches a source driver, receiving a clock signal ("CLK IN"), a display data ("DATA IN"), and a control signal ("START IN") to drive a display panel, comprising: a receiver (a combination of "input buffers 120, 121, 122, and 123") for receiving the clock signal ("CLK IN"), the display

data ("DATA IN"), and the control signal ("START IN"); and a transmitter (a combination of "counter 124", "clock control circuit 125", "data control circuit 126", "latch circuit 127", and "output buffers 128, 129, 130, and 131") coupled to the receiver, wherein **the transmitter enhances a driving ability of the clock signal ("CLK IN"), the display data ("DATA IN"), and the control signal ("START IN")** for use of another source driver in a next stage.

Examiner further states that Kumagai does not teach the features of "a transmitter receiving said master/slave setting signal, said transmitter responsive to said master/slave setting signal operating in one of a master mode and a slave mode; **wherein when said transmitter** operates in said master mode, **said transmitter** enhances a driving ability **of said clock signal, said display data, and said control signal for use of another source driver in a next stage; when said transmitter** operates in said slave mode, said transmitter directly outputs **said clock signal, said display data, and said control signal received from said receiver for use of said another source driver in said next stage.**"

Therefore, Examiner must think that the driving ability of the clock **signal** ("CLK IN"), the display data ("DATA IN"), and the control signal ("START IN") **are enhanced by the input buffers** 120, 121, 122, and 123 **and the output buffers** 128, 129, 130, and 131 **respectively, and then the enhanced signals are output** to the another source driver in the next stage. **In fact**, according to fig. 3 and par. [0103]-[0105] of Kumagai, **the input buffers** 120, 121, 122, and 123 and **the output buffers** 128, 129, 130, and 131 **respectively also enhance** the driving ability of the clock **signal** ("CLK IN"), the display data ("DATA IN"), and the control signal ("START IN") **for use of the another source driver in the next stage**.

Tough Examiner further states that Nakano (FIG. 4B and column 14, lines 23-28) teaches a transmitter (a combination of "timing control section 13b", "selector 13c", and "data output section 13d") of a source driver of a display, which operates in one of a master mode and a slave mode in responsive to a master/slave setting signal ("external control signal supplied to a control terminal 13h"), combination of the "timing control section 13b" and "selector 13c" of FIG. 4B of Nakano with FIG. 3 of Kumagai, the driving ability of the clock signal ("CLK IN"), the display data ("DATA IN"), and the control signal ("START IN") are **always enhanced by the input buffers** 120, 121, and 123 **respectively whatever whether the transmitter operates in a master/slave mode.**

Further, in Nakano (FIG. 4B, and column 14, lines23-28 and 45-48), the timing control section 13b **is switchable to an operation state or to a non-operation state** by the external control data signal, and the timing control section 13b **is used to generating the column electrode driving timing signal and the row electrode driving timing signal**. However, Nakano does not teach or suggest the timing control section 13b can enhance an input signal.

Accordingly, Kumagai in view of Nakano does not teach or suggest the features of "a transmitter, coupled to said receiver, transmitter receiving said master/slave setting signal, said transmitter responsive to said master/slave setting signal operating in one of a master mode and a slave mode; wherein when said transmitter operates in said master mode, said transmitter enhances a driving ability of said clock signal, said display data, and said control signal for use of another source driver in a next stage; when said transmitter operates in said slave mode, said transmitter directly outputs said clock signal, said display data, and said control signal received from said receiver for use of said

another source driver in said next stage", as claimed in claim 24.

In addition, Nakano (Figs. 3A, 3B and 4A, and column 12, lines 48-57) discloses the timing control section 13b for generating a driving a column electrode driving timing signal and a row electrode driving timing signal, and the row electrode driving timing signal is supplied to the row electrode driving circuit. Nakano (column 14, lines 29-37) discloses **one column electrode driving circuit 130 which is closest to the row electrode driving circuits 12 will be referred to as a "master column electrode driving circuit 130M"**. That is, in the plurality of column electrode driving circuits 130, **only one** column electrode driving circuit 130 which is closest to the row electrode driving circuits 12 **will be referred to as a "master column electrode driving circuit 130M".**

However, according to the Specification of the present invention, the operation mode of each source drivers of the claim 24 flexibly depends on the range of the acceptable system time delay. Taking a LCD panel with ten source drivers as an example, the possible combination of the source drivers can be M-M-M-M-M-M-M-M-M-M, M-S-M-S-M-S-M-S-M-S, M-S-S-M-S-S-M-S-S-S, M-S-S-S-M-S-S-S-M-S, or M-S-S-S-S-M-S-S-S-S; wherein M represents that the source driver operates in the master mode and S represents that the source driver operates in the slave mode. The above combination of the source drivers can be adjusted based on the resistance of the signal path. Hence, this embodiment can further reduce the power consumption and EMI.

Therefore, comparing with Kumagai in view of Nakano, the subject matter of claim 24 can produce new results.

Accordingly, claim 24 should be patentable over Kumagai in view of Nakano.

Claims 25-34 depends on the independent claim 24, and thus, should also be patentable.

Claim 35 recites "[a] flat panel display, ... a transmitter, coupled to said receiver, transmitter receiving said master/slave setting signal, said transmitter responsive to said master/slave setting signal operating in one of a master mode and a slave mode; wherein when said transmitter operates in said master mode, said transmitter enhances said driving ability of said clock signal, said display data, and said control signal for use of said another source driver in said next stage; when said transmitter operates in said slave mode, said transmitter directly outputs said clock signal, said display data, and said control signal received from said receiver for use of said another source driver in said next stage".

For the reasons similar to claim 24, claim 35 should be patentable over Kumagai in view of Nakano.

Claims 37-46 depends on the independent claim 24, and thus, should also be patentable.

CONCLUSION

For at least the foregoing reasons, it is believed that the pending claims 24-35 and 37-46 are in proper condition for allowance and an action to such effect is earnestly solicited. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,

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